IN THE SPECIFICATION:

Page 13, paragraphs 1 and 2, lines 2 - 19:

Fig. 6 is an exemplary circuit diagram of the pulse signal generating circuit 620 of Fig. 3. This circuit receives as inputs the power-on detect signal DET1 and signal SEL from power detect circuit 610 to generate pulse signals PUL1 and PUL2. Upon transition from 'Low' to 'High' of the DET1 signal, the half-pulse generators 622 and 623 generate initial pulses at half width (quarter cycle) to output through MUX 626 and MUX 627 the initial pulses of PUL1 and PUL2 with a pulse width equal to one half (½) of the pulse width of modulated audio signal APWM. Then, MUX 626 and MUX 627 are selected to pass through signals output from the 50:50 pulse generators 624 ~~and 625~~ in response to control signals from controllers 625, with duty cycle the same as system clock CLK and same period as pulse period signal PPS. According to an alternative embodiment, only one of the two half-pulse generators 622 and 623 is employed, depending on whether transistors 101, 301, 103, 301 are NMOS or PMOS type, to generate an initial half pulse at either PUL1 or PUL2.

Fig. 7(a) shows waveforms of the first detecting signal DET1 and the first and second pulse signals PUL1, PUL2 in case that the MOS transistors 101, 303, 103, 301 of Figs. 1 and 3 are NMOS transistors. It can be seen that signals PUL1 and PUL2 are opposite in phase at all times. Fig. 7(b) shows waveforms of the first and second pulse signals PUL1, PUL2 applicable when the MOS transistors 101, 303 of Figs. 1 and 3 are PMOS transistors and the MOS transistor 103, 301 are NMOS transistors. It can be seen that signals PUL1 and PUL2 are ~~opposite~~ in phase at all times.

IN THE DRAWINGS:

Amendment to Figure 6 is proposed to add the connection between the controller 625 and MUX 626 and 627. The insertion is shown in blue.